REMARKS/ARGUMENTS

Examiner J. Diaz is thanked for a complete search and thorough Office Action.

Reconsideration of the rejection of claims 18 and 19 under 35 U.S.C. 102(e) as being anticipated by Saitou et al. (U.S. Patent No. 5,739,546), reconsideration of the rejection of claim 20 as being unpatentable over Saitou et al. in view of Lou (U.S. Patent No. 5,759,906), and reconsideration of the rejection of claims 21-22 as being unpatentable over Saitou et al. is requested for the following reasons.

In Response to Arguments by the Examiner dated 10/21/03, page 3, the Examiner states in rebuttal that "However, nowhere in the claims applicant limited the formation of the fill layer to only the kerf area, as now argued."

The applicant wishes to point out to the Examiner that claim 18, element (a) states

> (a) a patterned conducting layer forming portions of semiconductor devices and a patterned fill layer in said kerf areas;

which is presented graphically in Figs. 6-8 and labeled 12A for the semiconductor devices in the chip area, and labeled 12B for the fill layer in the kerf area. As stated in claim 18 and clearly shown in Figs. 6-8, the patterned conducting layer and the fill layer are two separate, distinct layers after patterning, and do not form an electrical test

structure that is in both the device area and the kerf area, as in the cited prior art of Saitou et al. The applicant's invention is extendable to multilevels of metal layers, as shown in Fig. 8, which the prior art would fail to achieve.

The Examiner further states on page 3, "With regards to the arguments that the layer 6 of Saitou et al. is not a "fill layer" (page 3 of applicant's remarks), applicant should note that figure 2 of Saitou et al. shows a layer 6 filling the center of the kerf area (3)."

Saitou's layer 6 to which the Examiner refers is in the kerf area but does not fill the kerf area. As shown in Saitou's Fig. 2 and more clearly shown in Fig. 1, the layer 6 does not fill the kerf area. The Examiner is also referred to Saitou's Fig. 3, in which layer 6 is the same as layer 11, and as shown in Saitou's Fig. 1, layer 11 (6) extends from the kerf area into the chip area to form the Vss. This is not the applicant's invention.

Further, the Examiner states that the silicon oxide layer 7 is planar, as shown in Saitou's Fig. 3. This is not correct. In semiconductor technology it is important to provide a planar surface on a semiconductor substrate so that subsequent layers can be patterned using anisotropic etching techniques so that etch residue does not remain over steps in the underlying surface. The applicant's argument in the prior Response to Office Action is still valid. However, for the Examiner to understand the difference between a planar insulating layer and a conformal insulating layer, as is

commonly used in the semiconductor industry, Saitou's layer 7 (see Saitou's Fig. 3) and applicant's layer 16 (see applicant's Fig. 7) will now be described in detail.

In the semiconductor industry a planar layer remains planar over the edge of the underlying metal line, as depicted by insulating layer 16 over the metal line 12A in the applicant's Fig. 7. It is the applicant's fill layer 12B that achieves this planarity. In Saitou's Fig. 3 the insulating layer 7 drops down over the edge of the step of layer 6, and the difference in height is approximately equal to the thickness of the metal line 6. Because the thickness of Saitou's layer 7 over the metal line 6 and over the adjacent substrate area are the same, layer 7 is a conformal layer and is not planar. It is difficult to formulate an argument when the two structures (Saitou's and the applicant's) are so different. The applicant's structure is designed to form planar surfaces that are essential for forming multiple levels of integration for integrated circuits, while Saitou's invention is designed to build electrical test structures for testing devices on an integrated circuit. Therefore the applicant's invention could not be anticipated by Saitou et al. and further in view of Lou, and is patentable over Saitou et al. and in view of Lou.

It is requested that Examiner Jose R. Diaz call the undersigned Attorney at 845-452-5863 should there be anything that can be done to help bring this Patent Application to Allowance.

Respectfully submitted,

Stephen B. Ackerman

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